

FEATURES:

- 24-PIN DIP AND SURFACE MOUNTED PACKAGE
- 10:1 DELAY-TO-RISETIME RATION
- 20 EQUALLY-SPACE TAPS
- DELAY TIMES FROM 20-3000nS

ELECTRICAL CHARACTERISTICS:

Total Delay	:	20 to 3000nS
Tap Delays	:	5% Increments standard
Rise Time	:	10% Max of Total Delay
Characteristic Impedance	:	50 to 300Ω(±10%)
Attenuation	:	2dB Max
Distortion	:	±10% Max
Temperature Coefficient of Delay	:	100ppm/°C max
Operating Temperature Range	:	0°C to +70°C
Storage Temperature Range	:	-65°C to +130°C
Insulation Resistance	:	1000MΩ Min @50Vdc
Dielectric Strength	:	50Vdc

INPUT PULSE TEST CONDITION:

Pulse Voltage	:	2.5V
Pulse Width	:	5Td
Pulse Rise Time	:	2nS(10% to 90%)

YUAN DEAN SCIENTIFIC



Delay Line

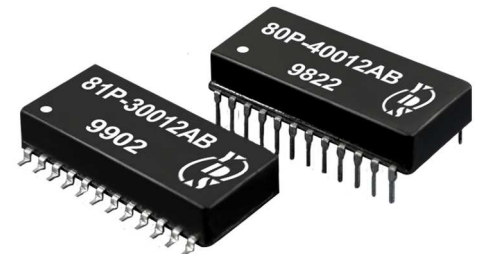
80P/81P SERIES

24 Pin

Dual In-Line

SOIC Surface Mounted

Passive



ELECTRICAL SPECIFICATIONS

PART NO.	Total Delay nS(± 5%)*	Tap Delay nS(±5%)**	Rise (nS)max	Impedance (Ω) (±10%)
80P/81P-02051XXNL	20	1	3	50
80P/81P-04051XXNL	40	2	4	50
80P/81P-06051XXNL	60	3	6	50
80P/81P-08051XXNL	80	4	8	50
80P/81P-10051XXNL	100	5	10	50
80P/81P-20051XXNL	200	10	20	50
80P/81P-02012XXNL	20	1	3	100
80P/81P-04012XXNL	40	2	4	100
80P/81P-06012XXNL	60	3	6	100
80P/81P-08012XXNL	80	4	8	100
80P/81P-10012XXNL	100	5	10	100
80P/81P-20012XXNL	200	10	20	100
80P/81P-30012XXNL	300	15	30	100
80P/81P-40012XXNL	400	20	40	100
80P/81P-50012XXNL	500	25	50	100
80P/81P-60012XXNL	600	30	60	100
80P/81P-80012XXNL	800	40	80	100
80P/81P-100012XXNL	1000	50	100	100
80P/81P-120012XXNL	1200	60	120	100
80P/81P-150012XXNL	1500	75	150	100
80P/81P-04022XXNL	40	2	4	200
80P/81P-06022XXNL	60	3	6	200
80P/81P-08022XXNL	80	4	8	200
80P/81P-10022XXNL	100	5	10	200
80P/81P-20022XXNL	200	10	20	200
80P/81P-30022XXNL	300	15	30	200
80P/81P-40022XXNL	400	20	40	200
80P/81P-50022XXNL	500	25	50	200
80P/81P-60022XXNL	600	30	60	200
80P/81P-80022XXNL	800	40	80	200
80P/81P-100022XXNL	1000	50	100	200
80P/81P-120022XXNL	1200	60	120	200
80P/81P-150022XXNL	1500	75	150	200
80P/81P-200022XXNL	2000	100	200	200
80P/81P-300032DDNL	3000	150	300	300

Note:

* or±2ns, whichever is greater.

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