FEATURES:

- INHERENT DELAY:15ns±1ns
- INPUT SIGNAL REQUIREMENTS:TTL LOGIC
- OUTPUT FAN-OUT:TTL SCHOTTKY LOAD
- TOTAL DELAY TOLERANCE:±5% OR ±1ns, WIG

YUAN DEAN SCIENTIFIC

Delay Line

90A SERIES

32 Pin

TTL Schottky

4-BIT

Programmable

ELECTRICAL CHARACTERISTICS:

I_{IH} Logic"1" Input Current	:	50uA max
I_{IL} Logic"0" Input Current	:	-2uA max
V_{OH} Logic"1" Output Voltage	:	2.4V min
V_{OL} Logic"0" Output Voltage	:	0.4V max
V_{IH} Logic"1" Input Voltage	:	2.0V min
V_{IL} Logic"0" Input Voltage	:	0.8V max
TA Operating Temperature	:	0℃ to 70℃
NH Fanout"1" Output	:	20 TTL Load
NL Fanout"0" Output	:	10 TTL Load
Supply Current	:	170mA Max

INPUT PULSE TEST CONDITION:

Pulse Voltage	:	3.0V
Pulse Width	:	3Td
Pulse Spacing	:	1000ns
Pulse Rise Time	:	2nS(0.75V to 2.4V)
Time Delay Measured	:	@1.5V level
Supply Voltage Vcc	:	5.0±0.25Vdc

ROHS COMPLIANT

TEL: 886-6-3842899 FAX: 886-6-3843288
E-MAIL: ydsweb@yds.com.tw

Rev: 0 2018/07/24

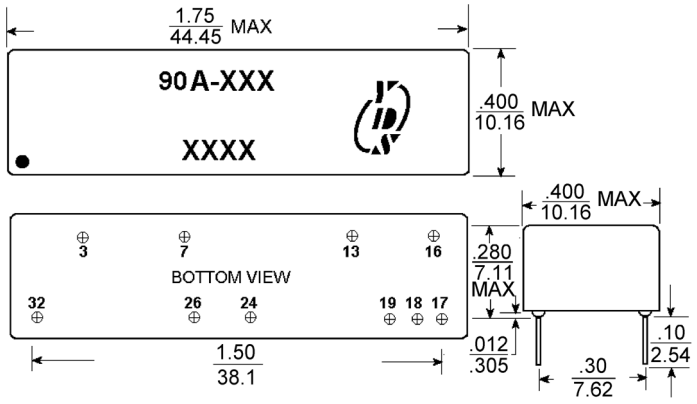
ELECTRICAL SPECIFICATIONS

PART NUMBER	INCREMENTAL DELAY PER STEP(ns)	TOTAL DELAY CHANGE(ns)
90A-015NL	1	15±1
90A-030NL	2	30±1.5
90A-045NL	3	45±2.2
90A-060NL	4	60±3
90A-075NL	5	75±3.7
90A-090NL	6	90±4.5
90A-120NL	8	120±6
90A-150NL	10	150±7.5
90A-180NL	12	180±9
90A-225NL	15	225±11.2
90A-300NL	20	300±15
90A-375NL	25	375±18.7
90A-450NL	30	450±22.5
90A-525NL	35	525±26.2
90A-600NL	40	600±30
90A-675NL	45	675±22.7
90A-750NL	50	750±37.5
90A-900NL	60	900±45
90A-1200NL	80	1200±60
90A-1500NL	100	1500±75

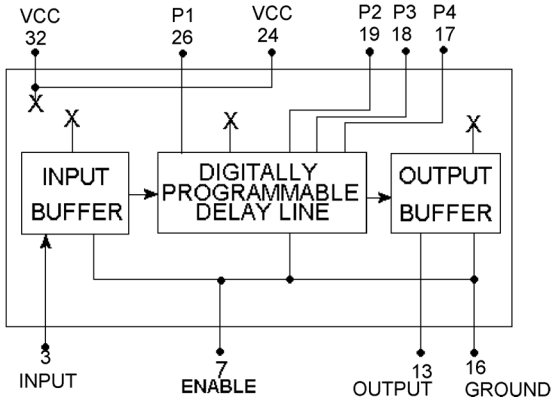
FUNCTION TABLE

ENABLE	ADDRESS(BIT NO.)				DEAY
L	L	L	L	L	T0
L	L	L	L	H	T1
L	L	L	H	L	T2
L	L	L	H	H	T3
L	L	H	L	L	T4
L	L	H	L	H	T5
L	L	H	H	L	T6
L	L	H	H	H	T7
L	H	L	L	L	T8
L	H	L	L	H	T9
L	H	L	H	L	T10
L	H	L	H	H	T11
L	H	H	L	L	T12
L	H	H	L	L	T13
L	H	H	H	L	T14
L	H	H	H	H	T15
H	X	X	X	X	L

Markings and Dimensions



Pin Connections



Dimensions: inches/mm

Unless otherwise specified, all tolerances are ±.010/±0.25

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