FEATURES:

- INHERENT DELAY(To):6ns TYPICAL
- 32-PIN DIP PACKAGE
- ECL INPUT AND OUTPUT LEVEL
- FAN-OUT 70 ECL CAPACITY

YUAN DEAN SCIENTIFIC

Delay Line

91A SERIES

32 Pin

ECL

4-BIT

Programmable

ELECTRICAL CHARACTERISTICS:

I_{IH} Logic"1" Input Current	:	265uA max
I_{IL} Logic"0" Input Current	:	0.5uA max
V_{OH} Logic"1" Output Voltage	:	-0.96V min
V_{OL} Logic"0" Output Voltage	:	-1.65V max
V_{IH} Logic"1" Input Voltage	:	-0.98V min
V_{IL} Logic"0" Input Voltage	:	-1.63V max
TA Operating Temperature	:	0℃ to 70℃
Supply Current	:	175mA TYP.

INPUT PULSE TEST CONDITION:

Pulse Voltage	:	1.0V(-0.75V to -1.75V)
Pulse Width	:	3Td
Pulse Spacing	:	10Td
Pulse Rise Time	:	2nS(20% to 80%V)
Time Delay Measured	:	@1.3V level
Supply Voltage Vcc	:	0Vdc
Supply Voltage Vee	:	-5.2Vdc

ROHS COMPLIANT

www.yds.com.tw
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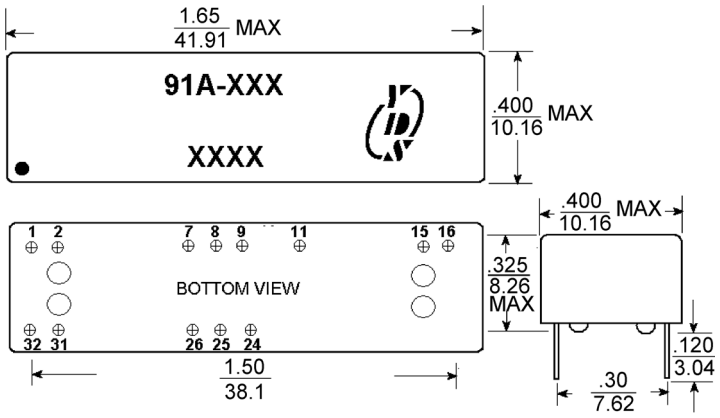
ELECTRICAL SPECIFICATIONS

PART NUMBER	INCREMENTAL DELAY PER STEP(ns)	TOTAL DELAY CHANGE(ns)
91A-015NL	1nS±0.5	15nS±1
91A-030NL	2nS±0.5	30nS±1.5
91A-045NL	3nS±0.5	45nS±2.2
91A-060NL	4nS±0.8	60nS±3
91A-075NL	5nS±1.0	75nS±3.7
91A-150NL	10nS±1.0	150nS±7.5
91A-300NL	20nS±2.0	300nS±15
91A-450NL	30nS±2.5	450nS±22.5
91A-600NL	40nS±3.0	600nS±30
91A-750NL	50nS±3.0	750nS±37.52

FUNCTION TABLE

ENABLE	ADDRESS(BIT NO.)				DEAY
L	L	L	L	L	T0
L	L	L	L	H	T1
L	L	L	H	L	T2
L	L	L	H	H	T3
L	L	H	L	L	T4
L	L	H	L	H	T5
L	L	H	H	L	T6
L	L	H	H	H	T7
L	H	L	L	L	T8
L	H	L	L	H	T9
L	H	L	H	L	T10
L	H	L	H	H	T11
L	H	H	L	L	T12
L	H	H	L	L	T13
L	H	H	H	L	T14
L	H	H	H	H	T15
H	X	X	X	X	L

Markings and Dimensions



Dimensions: inches/mm

Unless otherwise specified, all tolerances are ±.010/±0.25

Pin Connections